

**IN THE SPECIFICATION**

Please replace the Title the Invention currently on file with the following title:

**“Well Bias Voltage Control Circuit And Method”**

Please amend the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file as follows:

This application is a Continuation of nonprovisional application serial number 10/284,207 filed October 31, 2002, which was issued into U.S. Patent No. 6,653,890 on Nov. 25, 2003. Priority is claimed based on U.S. application No. 10/284,207 filed October 31, 2002, which claims the priority of Japanese application 2001-336208 filed on November 1, 2001.

Please amend the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file as follows:

In the second embodiment, in a manner similar to the first embodiment, the delay of the CMOS LSI can be compensated and the threshold voltage difference between the PMOS transistor and the NMOS transistor can be eliminated. In addition, by feeding back the signal vbap to the PN Vt balance compensation circuit 123, even if the threshold voltage difference occurs between the PMOS transistor and the NMOS transistor at the time of changing the signals vbap and vban in order to compensate delay, the difference can be compensated.